Docket No.: 08211/0200655-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Hidehiko Suzuki

Patent No.: 7,071,761

Issued: July 4, 2006

For: APPARATUS AND METHOD FOR REDUCING PROPAGATION DELAY

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.323 AND PATENT OFFICE MISTAKE (37 CFR 1.322)

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several errors which should be corrected.

The following errors were not in the application as filed by applicant:

In the Appication:

First Page Col. 2 (Other Publications), Line 3, Delete "htm>).*" and insert - - htm>.* - -.

First Page Col. 2 (Other Publications), Line 10, Delete "Piezolectric" and insert - - Piezoelectric - -.

First Page Col. 2 (Other Publications), Line 11, After "IGBT" insert - - GATE - -.

Column 2, Line 61, Delete "Of" and insert -- of --.

Column 4, Line 8 (Approx.), Delete "**11***R1," and insert - - **I1***R1, - -.

Column 4, Line 10 (Approx.), Delete "**11***R1," and insert - - **I1***R1, - -.

Enclosed please find marked up copies of List of References cited by examiner (1) page, Information Disclosure Statement (IDS) (1) page, and pages 3 and 5 of the Specification,

The errors were found in the application as filed by applicant. The errors now sought to be corrected are inadvertent typographical errors. The correction of which does not involve new matter or require reexamination.

First Page Col. 2 (Attorney, Agent or Firm), Line 1, Delete "PC;" and insert -- P.C.; --.

Column 3, Line 3, Delete "Vthr." and insert - - $V_{thr.}$ - -.

Column 5, Line 33, In Claim 1, delete "high power supply" before ", and where".

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to $300.00 or credit any excess in this fee to Deposit Account No. 04-0100. Payment of $100.00 is enclosed herewith.

Dated: September 19, 2006

Respectfully submitted,

By _____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,071,761
APPLICATION NO.	:	10/823,291
ISSUE DATE	:	July 4, 2006
INVENTOR(S)	:	Hidehiko Suzuki

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Application:

First Page Col. 2 (Other Publications), Line 3, Delete "htm>).*" and insert - - htm>.* - -.

First Page Col. 2 (Other Publications), Line 10, Delete "Piezolectric" and insert - - Piezoelectric - -.

First Page Col. 2 (Other Publications), Line 11, After "IGBT" insert - - GATE - -.

First Page Col. 2 (Attorney, Agent or Firm), Line 1, Delete "PC;" and insert -- P.C.; --.

Column 2, Line 61, Delete "Of" and insert -- of --.

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Column 4, Line 10 (Approx.), Delete "11*R1," and insert - - I1*R1, - -.

Column 5, Line 33, In Claim 1, delete "high power supply" before ", and where".

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Notice of References Cited	Application/Control No. 10/823,291	Applicant(s)/Patent Under Reexamination SUZUKI, HIDEHIKO	
	Examiner Thomas J. Hiltunen	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,242,973	06-2001	Kong et al.	327/589
	B	US-4,231,076	10-1980	Markarian et al.	361/512
	C	US-6,472,906	10-2002	Sanwo et al.	326/83
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	E	US-			
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	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	LESURF, JIM. The Scots Guide to Electronics. University of St. Andrews. [online], December 29, 2002. Retrieved from the Internet:< URL: http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm>).
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/08a/b (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/823,291
Filing Date	April 13, 2004
First Named Inventor	Hidehiko Suzuki
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	08211/0200655-US0/P05800

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA**	US-5,399,913-B1	03-21-1995	Widener et al.	

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Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. **CITE NO.: Those patent(s) or publication(s) which are marked with an double asterisk (**) next to the Cite No. are not supplied because they were previously cited by or submitted to the Office in a prior application relied upon in this application for an earlier filing date under 35 U.S.C. 120. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	B. Arntzen et al., "SWITCHED-CAPACITOR DC/DC CONVERTER WITH RESONANT GATE DRIVE", IEEE, 1996, pp. 414-420	
	CB	S.H. Wienberg, "A NOVEL LOSSLESS RESONANT MOSFET DRIVER", IEEE, 1992, pp. 1003-1010	
	CC	J.M. Bourgeois, "PCB BASED TRANSFORMER FOR POWER MOSFET DRIVE", IEEE, 1994, 99. 238-244	
	CD	D. Vasic et al., "A NEW METHOD TO DESIGN PIEZOELECTRIC TRANSFORMER USED IN MOSFET & IGBT GATE DRIVE CIRCUITS", IEEE, 2003, pp. 307-312	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

{S:\08211\0200655-US0\80011579.DOC}	Examiner Signature	Date Considered	

FIGURE 1 shows a block diagram of an embodiment of circuit 102. Circuit 102 includes voltage offset circuit 120 and logic circuit 130. Logic circuit 130 includes transistors M1 and M2.

In one embodiment, logic circuit 130 is a CMOS logic circuit. In other embodiments, logic circuit 130 may includes transistors other than MOSFET transistors, such as BJTs, and the like. In any case, transistor M1 is a p-type transistor, and transistor M2 is an n-type transistor. In one embodiment, logic circuit 130 includes an inverter circuit. In other embodiments, logic circuit 130 may be another type of logic circuit, such as a NAND gate, a NOR gate, and the like.

Instead of receiving identical inputs at the gates of transistors M1 and M2 like a standard CMOS inverter, logic circuit 130 is arranged to receive signal VPIN at the gate of transistor M1, and further arranged to receive signal VNIN at the gate of transistor M2. Logic circuit 130 is arranged to provide signal VOUT in response to signals VPIN and VNIN.

Additionally, voltage offset circuit 120 is arranged to provide signals VPIN and VNIN in response to signal VIN such that signal VNIN is offset relative to signal VPIN. Signal VNIN has a positive voltage offset relative to signal VIN. In one embodiment, signal VPIN has a negative voltage offset relative to signal VIN. In other embodiments, signal VPIN may be substantially the same as signal VIN.

FIGURE 2 illustrates a timing diagram of waveforms 201 and 203 of embodiments of signals VIN and VOUT respectively, for an embodiment in which signal VIN is a linearly increasing voltage ramp. Waveform 201 shows the voltage associated signal VIN over time, and waveform 203 shows the voltage associated with signal VOUT over time.

For an embodiment in which signal VIN is a linearly increasing voltage ramp, circuit 102 operates as follows. As shown in FIGURE 2, the voltage associated with signal VIN increases linearly over time. At time t_{thr}, the voltage associated with signal VIN reaches voltage V_{thr}, where V_{thr} is the threshold voltage of logic circuit 130. At time t_{thr}, logic circuit 130 reaches threshold. When logic circuit 130 is at threshold, V_{SG} of transistor M1 is substantially equal to V_{GS} of transistor M2. Also, when logic circuit 130 reaches threshold, signal VOUT changes from logic one to logic zero (i.e. from VDD to

components in timer circuit 300 of FIGURE 3, and may operate in a different manner in some ways. In timer circuit 400, voltage offset circuit 420 includes resistor circuit R1.

In operation, capacitor circuit C1 may be configured to provide signal VPIN in response to current I1 such that signal VPIN is a linearly increasing voltage ramp. Capacitor circuit C1 has a capacitance C.

Additionally, resistor R1 may be arranged to provide signal VNIN such that signal VNIN is substantially given by VPIN+I1*R1. In one embodiment, resistor circuit R1 is a single resistor. In other embodiments, resistor circuit R1 may include one or more resistors coupled together in series, in parallel, and the like.

When the threshold of inverter circuit 430 is reached, V_{SG} of transistor M1 is substantially equal to V_{GS} of transistor M2. Therefore, at the threshold of inverter circuit 130, VPIN may be substantially given by (VDD-I1*R1)/2, and VNIN may be substantially given by (VDD+I1*R1)/2. If resistor R1 were not included in timer circuit 400, then, at threshold, V_{SG} of transistor M1 and V_{GS} of transistor M2 would both be approximately VDD/2. By including resistor R1 in circuit 430, V_{SG} of transistor M1 and V_{GS} of transistor M2 are both approximately (I1*R1)/2 greater.

Additionally, VPIN(t) may be substantially given by I1*t/C1, where t is time, and where VPIN is substantially zero at time t=0. Also, VNIN(t) may be substantially given by I1*t/C + I1*R1.

Accordingly, the performance of circuit 400 may be roughly similar to that of a circuit that operates with a supply voltage of VDD+I1*R1, even though circuit 400 operates with a supply voltage of VDD. That is, circuit 400 has an "effective" supply voltage of roughly VDD+I1*R1. Employing resistor R1 in timer circuit 400 may substantially improve the stability circuit 400, as well as the propagation delay at low supply voltages.

FIGURE 5 shows a schematic diagram of an embodiment of timer circuit 500. Components in timer circuit 500 may operate in a similar manner to similarly named components in timer circuit 300 of FIGURE 3, and may operate in a different manner in some ways. In timer circuit 500, voltage offset circuit 520 includes capacitor C3. Also, timer circuit 500 includes capacitor C2 in place of capacitor C1 of FIGURE 3. Capacitor C2 may operate in a similar manner to capacitor C1 of FIGURE 3, and may operate in a